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Customer No.: 31561
Application No.: 10/707,874
Docket No.: 9945-US-PA-1

AMENDMENT

To the Claims:

Please amend claims as follows.

Claims 1-7 (canceled).

8. (currently amended) A method of fabricating a multi-bit flash memory, comprising:

providing a substrate;

forming a tunneling oxide layer on the substrate;

forming a conductive layer on the tunneling oxide layer;

forming an isolation layer in the conductive layer to partition the conductive layer into more than two conductive blocks arranged in an array with a plurality of rows extending from a region predetermined for forming one bit line to another region predetermined for forming another bit line and a plurality of columns, wherein each row comprises two conductive blocks, and each column comprises more than two conductive blocks;

forming a gate dielectric layer on the conductive layer;

patterning the gate dielectric layer and the conductive layer to form a floating gate comprising a predetermined number of conductive blocks arranged in an array having pluralities of rows and columns, wherein each row comprises a plurality of conductive blocks and each column comprises a plurality of conductive blocks, and wherein the patterned gate dielectric layer is formed vertically above said predetermined number of blocks arranged in said array;

forming the bit lines in the substrate at two sides of the floating gate;

forming a control gate on the floating gate so that each multi-bit cell of the multi-bit flash memory comprises said control gate, said patterned gate dielectric layer and said floating gate comprising said plurality of conductive blocks arranged in said array; and

performing a step of threshold voltage adjustment to result in different threshold voltages of the channel regions under the conductive blocks of different rows.

9. (original) The method according to Claim 8, wherein the material of the conductive layer comprises germanium polycide.

10. (original) The method according to Claim 8, wherein the step of forming the isolation region further comprises:

forming a patterned photoresist layer on the conductive layer to expose a part of the conductive layer predetermined for forming the isolation region;

performing an ion implantation step to implant dopant into the exposed conductive layer; and

performing an annealing process to react the dopant with silicon of the conductive layer to form the isolation region.

11. (original) The method according to Claim 10, wherein the dopant includes oxygen ions.

12. (original) The method according to Claim 11, wherein ion implantation step is performed with a dosage of dopant of about 1×10^{18} atoms/cm^2 to about 2×10^{18} atoms/cm^2.

13. (original) The method according to Claim 11, wherein the ion implantation step is performed with an implantation energy of about 20 KeV to about 80 KeV.

14. (original) The method according to Claim 10, wherein the dopant includes nitrogen ions.

15. (original) The method according to Claim 10, wherein the annealing process is performed at about 950°C to about 1150°C.

16. (original) The method according to Claim 8, further comprising a step of forming a field oxide layer after the step of forming the bit lines and before the step of forming the control gate.

17. (currently amended) A method of fabricating a multi-bit flash memory, comprising:

providing a substrate;

forming a tunneling oxide layer on the substrate;

forming a germanium polycide layer on the tunneling oxide layer;

forming a patterned photoreist layer on the germanium polycide layer, the patterned photoresist layer exposing a part of the germanium polycide layer predetermined for forming an isolation region;

performing an ion implantation step to implant dopant into the exposed germanium polycide layer;

performing an annealing process to react the dopant with silicon of the germanium polycide layer to form an isolation region that partitions the germanium polycide into more than two conductive blocks arranged in an array, the array having a plurality of rows extending from a region predetermined for forming a bit line to a region predetermined for forming another bit line and a plurality of columns each having said conductive

blocks;

forming a gate dielectric layer on the germanium polycide layer;

patterning the gate dielectric layer and the germanium polycide layer to form a floating gate comprising a predetermined number of conductive blocks arranged in an array having pluralities of rows and columns, wherein each row comprises a plurality of conductive blocks and each column comprises a plurality of conductive blocks, and wherein the patterned gate dielectric layer is formed vertically above said predetermined number of blocks arranged in said array;

forming the bit lines in the substrate at two sides of the floating gates ~~gate~~;

forming a control gate on the floating gate so that each multi-bit cell of the multi-bit flash memory comprises said control gate, said patterned gate dielectric layer and said floating gate comprising said plurality of conductive blocks arranged in said array; and

performing a step of threshold voltage adjustment to result in different threshold voltages of the channel regions under the conductive blocks of different rows.

18. (original) The method according to Claim 17, wherein the step of ion implantation further comprises implanting oxygen ions into the exposed germanium polycide layer.

19. (original) The method according to Claim 17, wherein the step of ion implantation further comprises implanting nitrogen ions into the exposed germanium polycide layer.

20. (original) The method according to Claim 17, further comprising forming a field oxide and a spacer on a sidewall of the floating gate after the step of forming the bit lines and before the step of forming the control gate.